WHAT IS CLAIMED IS:

1. A computer system comprising a CPU for operating with pipeline processing, a ROM storing a program to be executed by said CPU, and at least one ROM correction unit including a fist storage unit for storing a subject address of an original instruction group in the program having a bug therein, a second storage unit for storing a modified instruction group for replacing the original instruction group by the modified instruction group having a branch address, a comparator for comparing a current address of a current instruction read from said ROM against the subject address, a selector for selecting the current address or the branch address based on a result of the comparison by said comparator, and a flag generator for setting a ROM correction flag when said selector selects the branch address.

2. The computer system as defined in claim 1, wherein said at least one ROM correction unit include a plurality of ROM correction units.

3. The computer system as defined in claim 1, wherein said flag is set at an execution stage of a branch instruction indicating the current address to jump to said branch address.

4. The computer system as defined in claim 1, wherein the modified instruction group is supplied from outside the computer system.